2007 Symposium on Nano Device Technology

The Symposium on Nano Device Technology 2007 organized by National Nano Device NARL, will provide an open forum for the discussion of recent developments on nano-technology and advanced devices, materials and processes. Scientists, scholars and experts in the fields

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NDL National Nano Device Laboratories 國家奈米元件實驗室

時間: 中華民國96年5月9 - 15日
地點: 新竹市科學工業園區展業一路26號 奈米電子研究大樓 國際會議廳

奈米元件技術研討會 2007

主題
》後矽奈米電子元件技術．
》奈米生物技術．
》功能性奈米材料技術．
》奈米檢測技術．
》高頻技術及應用．
》奈米光晶元件技術

HF Characterization of Silicon Devices - with Special Emphasis on NWA Calibration and De-embedding Verification

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ABSTRACT

Characterizing silicon devices has become more challenging due to the improved speed performance of modern technologies. This implies the need to pay more attention to accurate High Frequency (HF) characterization measurements and especially to reliable verification procedures. This includes verifying the network analyzer calibration quality and ensuring that the correct HF signal level is applied to the components, in order to avoid unrealistic S-parameter measurements. Another important topic is an accurate de-embedding. For on-wafer measurements, the measurement results of the de-embedding dummy structures should be verified first, before the diodes or the transistors can be de-embedded from these parasitics. The final challenge for nonlinear devices is to combine the HF measurements with consistent DC measurements, considering for example different self-heating effects during DC and S-parameter measurements. This paper will give an overview about practical methods to obtain reliable and accurate HF measurement results, how to interpret S-parameter curves, and how to inspect the S-parameter data with underlying standard circuit schematics.

Toe-Naing SWE received his bachelor of engineering in 1995, and pursued his Master's degree at the Nanyang Technological University (NTU, Singapore) in 1999. He continued his research work in NTU for 3 years, working on characterization and modeling of deep submicron devices for system-on-a-chip applications.

Toe-Naing acquired extensive experience with RFIC technologies, ranging from semiconductor physics, device and test structure design, characterization and modeling of active/passive devices. Prior to his employment with Agilent Technologies, he characterized and modeled the processes of 3 major silicon foundries in Asia/Europe.

Toe-Naing joined the Agilent Modeling Center in Jan 2001 and is one of the key members of the technical delivery team. He is responsible for the parameter extraction of noise parameters, spiral inductor models, BSIM3/4, PSP, BSIMSOI, MEXTRAM, HICUM and other industry standard models.

Toe-Naing specializes in high frequency measurement, involving network analyzers, parametric sources, precision impedance analyzers and noise parameter measurement systems. He has extensive experience with various device modeling softwares, especially Agilent's IC-CAP and SPICE-based simulators.