

2007 Symposium on Nano Device Technology

The Symposium on Nano Device Technology 2007 organized by National Nano Device Laboratories (NNDL) will provide an open forum for the discussion of recent developments on nano-technology and advanced devices, materials and processes. Scientists, scholars and experts in the fields

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 **NNDL** National Nano Device Laboratories
國家奈米元件實驗室



時間: 中華民國96年5月9-15日

地點: 新竹市科學工業園區展業一路26號 奈米電子研究大樓 國際會議廳

奈米元件技術研討會 2007

主題

- 》後矽奈米電子元件技術
- 》奈米生物技術
- 》功能性奈米材料技術
- 》奈米檢測技術
- 》高頻技術及應用
- 》奈米光晶元件技術

MOSFET Reliability Modeling and Simulation Technology

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ABSTRACT

The continuous CMOS technology advancement essentially requires a device-level reliability modeling solution and a circuit-level reliability simulation solution which can be used in both the technology development qualification and design for reliability. In this talk, a practical reliability modeling and simulation technology based on the BSIMProPlus and RelXpert tools is discussed in details. The major reliability effects are focused on the NBTI and HCI, and their analytical models are physically described. The reliability model implementation in BSIMProPlus and RelXpert tools based on the novel AgeMOS concepts are also illustrated. It is critical to be able to accurately extract the physical NBTI and HCI reliability models which may not be possible without careful design of the stress experiments, understanding of the reliability effects, the efficient extraction and optimization, and the model QA flows. The reliability model tool like BSIMProPlus is designed for this purpose and is linked to Cadence's reliability simulator called RelXpert seamlessly and efficiently.

James Ma received his BS and MS degrees from South China University of Technology, China, in 1986 and 1989 respectively, and his Ph.D. degree from University of Hong Kong in 1992, all in electrical engineering. He was a postdoctoral researcher in the EECS Dept. of UC Berkeley from 1992 to 1994, working for Profs. Ping Ko and Cheming Hu.

In 1994 ~ 1997 and 1998 ~ 2005, he worked for Integrated Device Technology Inc., USA, as a senior device engineer and manager, responsible for CMOS device development, device modeling, and test chip design. From 1997 to 1998, he worked for Chrontel Inc., USA, as a device technology manager. In 2005 ~ 2006, he worked for Cadence Design Systems Inc., as a senior engineering manager in charge of the worldwide device modeling service and product engineering for BSIMProPlus and NoisePro.

In late 2006, he and his colleagues found the ProPlus Design Solutions Inc. in California, USA, which specializes in advanced device modeling tool and modeling services. Soon after, his company acquired the BSIMProPlus and NoisePro product lines from Cadence, including the Advanced Modeling Service Lab. He then became the President and CEO of the company. He has published ~45 technical papers in international conferences and journals. He holds one US patent and has a few more in pending.