

2007 Symposium on Nano Device Technology

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NDL National Nano Device Laboratories
國家奈米元件實驗室



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地點: 新竹市科學工業園區展業一路26號 奈米電子研究大樓 國際會議廳

奈米元件技術研討會 2007

主題

- 》後矽奈米電子元件技術
- 》奈米生物技術
- 》功能性奈米材料技術
- 》奈米檢測技術
- 》高頻技術及應用
- 》奈米光晶元件技術

Physical Layout Design Optimization of Spiral Inductors for Silicon-Based RFIC Applications

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ABSTRACT

Designing spiral inductors with the constraint of generating similar inductance values is used to investigate quantitatively how physical layout design parameters such as core diameter, conductor spacing and width would affect their performance. The experimental results in this paper reveal that inductors' core diameters must be adequately large, more than 100 μm , to ensure high quality factor characteristics and their conductor spacing should be minimal to obtain larger per unit area inductance value. A novel design methodology which optimizes the conductor width of inductors allows alignment of its peak quality factor to the circuit's operating frequency, enhancing the gain, input/output matching characteristics and noise figure of a giga-hertz amplifier.

Choon Beng received the B.E. (Hons) (Elect) and M.E. (Elect) from Nanyang Technological University (NTU), Singapore, in 1999 and 2001 respectively. From 2001 to 2006, he worked in Chartered Semiconductor Manufacturing Ltd as a Device Modeling Engineer and in Advanced RFIC (S) Pte Ltd's Device Modeling group as the Engineering Manager. He currently supports Cascade Microtech Inc.'s Asia Pacific operations in the area of application engineering and concurrently, he is completing his doctorate degree in NTU. His research interests include design, characterization and modeling of silicon-based devices for RFIC Applications. He currently has 9 patents granted with several others pending.