

2007 Symposium on Nano Device Technology

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國家奈米元件實驗室



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地點: 新竹市科學工業園區展業一路26號 奈米電子研究大樓 國際會議廳

奈米元件技術研討會 2007

主題

- 》後矽奈米電子元件技術
- 》奈米生物技術
- 》功能性奈米材料技術
- 》奈米檢測技術
- 》高頻技術及應用
- 》奈米光晶元件技術

Validation of on-wafer Vector Network Analyzers

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ABSTRACT

This paper applies a known vector network analyzer comparison technique to an on-wafer measurement environment. The purpose is to investigate and expand upon this technique's applicability for use in validating an on-wafer VNA system of unknown accuracy by comparing it to an on-wafer VNA system of trusted accuracy. The technique involves taking calibrated S-Parameter measurements with each system over a set of validation devices and calculating the measurement differences between the two systems. These differences are then compared to the estimated repeatability uncertainty bounds of the two VNAs in order to validate or invalidate the unknown system's capabilities. Results and limitations of this procedure are discussed.

Choon Beng received the B.E. (Hons) (Elect) and M.E. (Elect) from Nanyang Technological University (NTU), Singapore, in 1999 and 2001 respectively. From 2001 to 2006, he worked in Chartered Semiconductor Manufacturing Ltd as a Device Modeling Engineer and in Advanced RFIC (S) Pte Ltd's Device Modeling group as the Engineering Manager. He currently supports Cascade Microtech Inc.'s Asia Pacific operations in the area of application engineering and concurrently, he is completing his doctorate degree in NTU. His research interests include design, characterization and modeling of silicon-based devices for RFIC Applications. He currently has 9 patents granted with several others pending.